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<u>L14</u>	(712/230-248)[CCLS]	3464	<u>L14</u>
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<u>L5</u>	(prefetch\$6 or fetch\$7) near10 (simultaneous\$4 or parallel\$5 or concurrent\$4)	6952	<u>L5</u>
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<u>L3</u>	L1 and (map\$5 or associat\$4 or allocat\$5 or deallocat\$5) near8 (memor\$4 or space or region\$1 or section\$1 or range\$1 or area\$1 or location\$1 or block\$1 or segment\$1) NEAR55 VOLATILE	63	<u>L3</u>
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IEEE JNL IEEE Journal or Magazine

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IET JNL IET Journal or Magazine

1. Simultaneous subordinate microthreading (SSMT)

Chappell, R.S.; Stark, J.; Kim, S.P.; Reinhardt, S.K.; Patt, Y.N.;

[Computer Architecture, 1999. Proceedings of the 26th International Symposium on](#)
2-4 May 1999 Page(s):186 - 195

Digital Object Identifier 10.1109/ISCA.1999.765950

[AbstractPlus](#) | Full Text: [PDF\(116 KB\)](#) IEEE CNF[Rights and Permissions](#)

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

2. The impact of incorrectly speculated memory operations in a multithreaded architecture

Sendag, R.; Ying Chen; Lija, D.J.;

[Parallel and Distributed Systems, IEEE Transactions on](#)

Volume 16, Issue 3, Mar 2005 Page(s):271 - 285

Digital Object Identifier 10.1109/TPDS.2005.36

[AbstractPlus](#) | Full Text: [PDF\(1616 KB\)](#) IEEE JNL[Rights and Permissions](#)**3. Using incorrect speculation to prefetch data in a concurrent multithreaded processor**

Ying Chen; Sendag, R.; Lija, D.J.;

[Parallel and Distributed Processing Symposium, 2003. Proceedings. International](#)

22-26 April 2003 Page(s):9 pp.

Digital Object Identifier 10.1109/IPDPS.2003.1213177

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Chappell, R.S.; Tseng, F.; Yoaz, A.; Patt, Y.N.;

[Microarchitecture, 2002. \(MICRO-35\). Proceedings. 35th Annual IEEE/ACM International Symposium](#)

18-22 Nov. 2002 Page(s):74 - 84

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Huiyang Zhou;
Computer Architecture Letters, IEEE
Volume 5, Issue 1, Jan.-June 2006 Page(s):22 - 25
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7. The Speculative Prefetcher and Evaluator Processor for Pipelined Memory Hierarchies
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8. Slipstream execution mode for CMP-based multiprocessors
Ibrahim, K.Z.; Byrd, G.T.; Rotenberg, E.;
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9. TCP: tag correlating prefetchers
Hu, Z.; Martonosi, M.; Kaxiras, S.;
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10. Reducing branch delay to zero in pipelined processors
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12. Transparent threads: resource sharing in SMT processors for high single-thread performance
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